CBCS SCHEME

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18CS34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, analyze the basic operational concepts of a computer. Give the operating steps. **(10 Marks)**

b. Explain Big Endian and little Endian assignment. Consider a computer that has a byte addressable memory organized in 32 WORDS, according to a Big Endian scheme. A program reads ASCIL characters entered at a keyboard and store them in successive byte location starting at 3000. Show how the contents of 3 memory words at location 3000, 3004 and 3008 after the string "VTU BELAGAVI" has been entered.
(ASCII codes : V = 56H, T = 54H, U = 55H, " " = 20H, B = 42H, E = 45H, L = 4CH, A = 41H, G = 47H, I = 49H) **(10 Marks)**

OR

2 a. Define an addressing mode. Explain any 4 types of addressing modes with suitable example. **(10 Marks)**

b. Register R_1 and R_2 of computer contains the decimal values 1200 and 4600. What is effective address of the memory operand in each of following instructions :

(i) LOAD $20(R_1)$, R_5
(ii) MOVE #3000, R_5
(iii) SUBSTRACT $(R_1)+$, R_5
(iv) STORE $30(R_1, R_2)$, R_5
(v) ADD $-(R_2)$, R_5 **(05 Marks)**

c. Explain logical shift instructions with examples. **(05 Marks)**

Module-2

3 a. List the difference between memory mapped I/O and I/O mapped I/O. **(04 Marks)**

b. With neat sketches, explain various methods for handling multiple interrupts requests raised by multiple devices. **(08 Marks)**

c. With neat diagram, explain centralized bus arbitration and distributed bus arbitration. **(08 Marks)**

OR

4 a. Explain the I/O interface for an input device to the processor with a neat block diagram. **(08 Marks)**

b. With neat diagram, explain synchronous bus transfer during an input operation. **(06 Marks)**

c. Explain the tree structure of USB with split bus operation. **(06 Marks)**

Module-3

5 a. Explain the organization of 1K*1 memory chip. **(06 Marks)**

b. With neat diagram, explain the internal organization of 2M*8 dynamic memory chip. **(10 Marks)**

c. Explain the memory hierarchy with respect to speed, size and cost. **(04 Marks)**

OR

6 a. Design a memory organization of 2M*32 memory module using 512K*8 static memory chips and explain the same. **(08 Marks)**

b. Illustrate the cache mapping techniques. **(06 Marks)**

c. Calculate the average access time experienced by a processor, if cache hit rate is 0.88, Miss penality is 0.015 ms and cache access time 10 ms? **(06 Marks)**

Module-4

7 a. Convert the following pairs of decimal numbers to 5 bit, signed 2's complement, binary numbers and add them. State whether or not overflow occurs in each case :
(i) 6, 10 (ii) −3,−8 (iii) −10,−13 (iv) −14,11 **(10 Marks)**

b. Describe the principle of carry-look Ahead addition for 4-bit adder circuit, built using B-cells and calculate the number of gate delays for S_3 and C_4. **(10 Marks)**

OR

8 a. Explain Booth multiplication algorithm. Apply the same to multiply signed number −13 and 9. **(08 Marks)**

b. Perform the division of numbers 8 by 3 (8÷3) using Restoring Division Method. **(08 Marks)**

c. Design a logic circuit to perform addition / substraction of 2n-bit numbers X and Y. **(04 Marks)**

Module-5

9 a. Illustrate the sequence of operations required to execute the instruction ADD (R_3), R_1 on a single Bus processor. **(10 Marks)**

b. Explain the 3 Bus organization of a data path with a neat diagram. **(10 Marks)**

OR

10 a. With neat diagram, explain the microprogrammed control method for design of control unit and write the micro-routine for instruction BRANCH < 0. **(10 Marks)**

b. Bring out the difference between micro programmed and Hard wired control. **(04 Marks)**

c. With neat diagram, explain 4-stage pipeline. **(06 Marks)**

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